جامعة الملك عبدالله
للعلوم والتقنية
King Abdullah University of
Science and Technology

Course Syllabus: VLSI Design - EE 201

Division	Computer, Electrical and Mathematical Sciences & Engineering
Course Number	EE 201
Course Title	VLSI Design
Academic Semester	Summer
Academic Year	2016/2017
Semester Start Date	06/04/2017
Semester End Date	08/03/2017
Class Schedule (Days & Time)	03:00 PM - 06:00 PM | Mon Thu

Instructor(s)

Name	Email	Phone	Office Location	Office Hours
Hossein Fariborzi	hossein.fariborzi@kaust.edu.sa	+966128087302	3275, 3, Ibn Sina (bldg. 3)	12:30-2 Sundays, or with prior appointment

Teaching Assistant(s)

Name	Email

Course Information

Comprehensive Course Description	This course is an Introduction to CMOS VLSI Design. The following topics will be covered: –Foundation: CMOS device operation as a digital switch, manufacturing process, wire/interconnect models –Circuit perspective: Logic gates (NAND, NOR, XOR, etc), combinational and sequential logic blocks and functional units (flops, adders, shifters, multipliers, registers) –System perspective: Implementation strategies, architecture of memory arrays and datapath -Design trade-offs and compromises: Speed, energy consumption, area, cost
Course Description from Program Guide	Design techniques for rapid implementations of very large-scale integrated (VLSI) circuits, MOS technology and combinational and sequential logic. Structured design. Design rules, layout design techniques. Computer Aided Design (CAD): layout, design rule checking, logic and circuit simulation, timing and power analysis.
Goals and Objectives	In this course students will learn how to analyze and design CMOS digital circuits and optimize them with respect to different constraints such as size (cost), speed, power dissipation. Mastery of design trade-offs and application of these concepts in a design mini-project is the ultimate goal of this course.
Required Knowledge	- Knowledge of basic logic operations -Fundamentals of CMOS operation
Reference Texts	–Digital Integrated Circuits: Rabaey et al (2nd ed) –CMOS VLSI Design: Weste et al (4th ed)
Method of evaluation	**30.00**% - Final exam **20.00**% - Research Project **10.00**% - Quiz(zes) **20.00**% - Midterm exam **20.00**% - Homework /Assignments

Nature of the assignments	3 Homework/Assignments: Analysis, Design and Simulation Problem sets One literatute review and class presentation assignment One Mini-project: An extension/enhancement of one of the major architectures in the course
Course Policies	- 20% deduction per day for any late homework submission - Late submission for project or literature survey won't be accepted
Additional Information	

Tentative Course Schedule
(Time, topic/emphasis & resources)

Week	Lectures	Topic
1	Mon 06/05/2017 Thu 06/08/2017	Introduction: CMOS operation, Inverter
2	Mon 06/12/2017 Thu 06/15/2017	Combinational Logic Design
3	Mon 06/19/2017 Thu 06/22/2017	Sequential Logic Design
4	Mon 06/26/2017 Thu 06/29/2017	No class (Eid break)
5	Mon 07/03/2017 Thu 07/06/2017	Wire/Interconnect Midterm exam
6	Mon 07/10/2017 Thu 07/13/2017	Timing in digital circuits Arithmetic Units
7	Mon 07/17/2017 Thu 07/20/2017	Memories and array structures
8	Mon 07/24/2017 Thu 07/27/2017	Case study, literature survey and project presentations
9	Mon 07/31/2017 Thu 08/03/2017	Literature Survey, project presentations and final exam
10		NA
11		NA
12		NA
13		NA
14		NA
15		NA
16		NA
17		NA
18		NA

Note

The instructor reserves the right to make changes to this syllabus as necessary.