جامعة الملك عبدالله
للعلوم والتقنية
King Abdullah University of
Science and Technology

Course Syllabus: Integrated Analog/Digital Interface Circ - EE 302

Division	Computer, Electrical and Mathematical Sciences & Engineering
Course Number	EE 302
Course Title	Integrated Analog/Digital Interface Circ
Academic Semester	Summer
Academic Year	2017/2018
Semester Start Date	06/10/2018
Semester End Date	08/09/2018
Class Schedule (Days & Time)	09:00 AM - 12:00 PM | Mon , 01:00 PM - 04:00 PM | Thu

Instructor(s)

Name	Email	Phone	Office Location	Office Hours
Hossein Fariborzi	hossein.fariborzi@kaust.edu.sa	+966128087302	3275, 3, Ibn Sina (bldg. 3)	Thu 4-5 PM Mon 1-2 PM

Teaching Assistant(s)

Name	Email

Course Information

Comprehensive Course Description	This course covers most of the well-known digital-to-analog and analog-to-digital conversion schemes. These include the flash, folding, multi-step and pipeline Nyquist rate architectures. Oversampling, sigma-delta converters are also discussed. Intensive literature review on the current converters and practical design in the framework of a course project is a significant part of this course. Students design (schematic and layout) and simulate (pre- and post-layout) complete converters with strict FOM requirements. The course is offered in 5 main modules: -Overview of main concepts and definitionsclassic DAC/ADC architectures -Sub-circuits and building blocks of data converters: voltage comparators and switched capacitor circuits -Flash, SAR and ADCs -Advanced ADC and DAC architectures and trends -Study of major Figure of Merits and the path toward the improvement of current architectures
Course Description from Program Guide	This course covers most of the well-known digital-to-analog and analog- to-digital conversion schemes. These include the flash, folding, multi- step and pipeline Nyquist rate, architectures. Oversampling converters are also discussed. Practical design work is a significant part of this course. Students design and model complete converters.
Goals and Objectives	The students will be able to: -Comprehend the basic principles and challenges in data converter design -Combine the knowledge acquired in the lectures and recent literature and design an optimized ADC, targeting improvement of (at least) one of the major FOMs.
Required Knowledge	The main requirement is knowledge of CMOS analog/mixed-signal circuit design. Either EE 202 or EE 201 is sufficient. A big bonus would be prior design experience with Cadence tools.

Reference Texts	The main reference is the lecture notes, but the following books are suggested, all of them accessible from KAUST library e-collection: -CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters, Rudy van de Plassche. http://link.springer.com/book/10.1007%2F978-1-4757-3768-4 -Advanced Data Converters, Gabriele Manganaro http://ebooks.cambridge.org/ebook.jsf?bid=CBO9780511794292 -Principles of Data Conversion System Design, B. Razavi. -Data Converters, F. Maloberti. -Analog-to-Digital Conversion, M. Pelgrom.
Method of evaluation	**40.00**% - Course Project(s) **15.00**% - Scientific review article presentation **15.00**% - Quiz(zes) **30.00**% - Final exam
Nature of the assignments	As the lectures progress, the students will review the state-of-the-art architectures and after consulting with the instructor, present their critical evaluation of 3-5 designs in the class. Active participation in the discussions is of key importance. The course project is an individual effort, and requires students to use their newly acquired knowledge to design an advanced ADC from A to Z.
Course Policies	20% penalty for each day of late submission, for all assignments and projects. Missing a class is a bad idea. If you really HAVE TO miss one class, make sure you sit down with the instructor to discuss the content and get a make-up reading assignment.
Additional Information	

Tentative Course Schedule *(Time, topic/emphasis & resources)*		
Week	**Lectures**	**Topic**
1	Mon 06/11/2018 Thu 06/14/2018	Introduction, basic concepts and definitions, standard and traditional ADC/DAC categories and architectures. No class on Thursday 6/14 due to the Eid holidays.
2	Mon 06/18/2018 Thu 06/21/2018	No classes- Eid Holidays
3	Mon 06/25/2018 Thu 06/28/2018	Monday: Class presentation and discussion 1, Classic ADCs and DACs Thursday (Lecture): Classic converters (part 2) Data converters terminology, errors and non-idealities
4	Mon 07/02/2018 Thu 07/05/2018	ADC Errors, SNR, SINAD Pipeline ADC Sampling concepts, Aliasing and Nyquist Theorem
5	Mon 07/09/2018 Thu 07/12/2018	Monday: Class presentation and discussion 2, SAR and pipeline ADCs Thursday (Lecture): Time interleaved ADCs, Oversampling and Delta-Sigma ADCs
6	Mon 07/16/2018 Thu 07/19/2018	Monday (Lecture): Self Calibration in ADCs, Current-based and oversampling DACs Thursday: Class discussion and presentation 3, Potential designs for final project
7	Mon 07/23/2018 Thu 07/26/2018	Monday: In depth literature review of the potential architectures, selection of an architecture for the final project after class discussion Thursday: Project update checkpoint (class discussion): initial simulation results
8	Mon 07/30/2018 Thu 08/02/2018	Monday: Final simulation results discussion. Initial layout design checkpoint Thursday: Final layout design. Class discussion on optimization of layout. Pre and post-layout simulation comparison
9	Mon 08/06/2018 Thu 08/09/2018	Final Exam on Monday 8/6/2018 Project presentation: 8/9/2018
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Note

The instructor reserves the right to make changes to this syllabus as necessary.